A CMOS dynamic random access architecture for RF readout of quantum devices

Delft 1/05/2019

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Quantum Computers use basic concepts from Quantum Mechanics…

\[ |\psi\rangle = \cos(\theta/2)|0\rangle + \sin(\theta/2)e^{i\varphi}|1\rangle \]
Superposition

\[ |\psi\rangle = \frac{1}{\sqrt{2}}(|10\rangle - |01\rangle) \]
Entanglement

…and uses them to obtain computational speed-up wrt conventional compt.

Factorisation

\[ \psi = c |0\rangle + s |1\rangle \]

Database searches

\[ |\psi\rangle = \frac{1}{\sqrt{2}}(|10\rangle - |01\rangle) \]

Optimisation

\[ |\psi\rangle = \cos(\theta/2)|0\rangle + \sin(\theta/2)e^{i\varphi}|1\rangle \]

P. Shor, SIAM J. Compt 26 1484


Qubits

IBM Quantum Experience (2016)


IonQ (2018)
# Silicon Quantum Processors - Specs

<p>| | | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td><strong>First demonstrations</strong></td>
<td>2012</td>
<td>Maune Nature Morello, Nature</td>
</tr>
<tr>
<td><strong>Single Qubit Gates</strong></td>
<td>&gt;99.9%</td>
<td>Yoneda et al Nat Nano 13 102 (2018)</td>
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<tr>
<td><strong>Two Qubit Gate</strong></td>
<td>98%</td>
<td>W. Huang et al arXiv:1805.05027 (2018)</td>
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</table>
Opportunities at the device level

- For Control
  Utilize MW cavities

- For Readout
  Gate-based sensing
  + Pauli Spin Blockade

- For Quantum Dot definition
  Geometrically defined
  (Silicon Nanowires)

UNSW (2018)
Opportunities at the circuit level

One or two qubits

Large scale quantum circuits

Interfaces with classical electronics

Veldhorst, Nature Nano. 9 981 (2014)
Kawakami, Nat Nano 9 (2014)
Maurand, Nat Commun 7 (2016)

Veldhorst, Nat. Commun. 8 1766 (2017)
Vandersypen, NPJ Quant. Info 3 34 (2017)
Classical – Quantum Interfaces

Large-scale Quantum Computing

1 QUBIT -> 1 LINE
Classical – Quantum Interfaces

Large-scale Quantum Computing

N QUBIT \rightarrow O(N^{1/p}) \text{ LINES}
\quad p = \text{Rent Exponent}
DRAM applied to Quantum Devices?

Classical DRAM (p=2)

DRAM for QDs?

Memory Capacity  1GB
Refresh Time  64 ms
Capacitance  ~1 fF
Leakage current  ~1-10 fA
Our Response

- A transistor-based solution
  - QDs on narrow FDSOI
  - Control FET on wide FDSOI

- Focused on Readout
  - Sequential gate-based readout
  - Mixed (Analogue-Digital) signals

- Advantage
  - One resonator per row
  - Shared control via dataline

- Modular approach
  - Test 1 cell
  - Test 2 cells (sequential readout)

Our Response

- Time-multiplexing in the row
- Freq-multiplexing in the column
A CMOS dynamic random access architecture for RF readout of quantum devices
3D Fully-depleted silicon-on-insulator FET

$V_{tg}$

$V_{sd}$

200 nm

$|\Psi|^2 (\times 10^{-3} \text{ nm}^{-3})$

$y (\text{nm})$

$z (\text{nm})$

$|\Psi|^2 (\times 10^{-3} \text{ nm}^{-3})$

$y (\text{nm})$

$z (\text{nm})$

D. Ibberson et al., APL 113 053104 (2018)
Can we operate a single cell at mK using FDSOI?

**FET:**
- Width=10 um
- Length=50 nm

**QD:**
- Width=60 nm
- Length=30 nm

Can we operate a single cell at mK using FDSOI?
- Can we perform RF readout via the control FET?
- How sensitively?
- Can we lock charge?

FET:
Width=10 μm
Length=50 nm

QD:
Width=60 nm
Length=30 nm

CMOS technology
Devices are on same chip at mK

Single-electron memory cell

**FET:**
- Width=10 µm
- Length=50 nm

**QD:**
- Width=60 nm
- Length=30 nm

**CMOS technology**
Devices are on same chip at mK

Single-electron memory cell – WL

Single-electron memory cell

Two Cells
Two cells – Frequency spectrum


Spectral overlap
13 MHz

Quality factor
100->40
Two cells - Reflectometry

Digital inputs and variability

<table>
<thead>
<tr>
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<th>Cell 1 ($V_{WL1}$)</th>
<th>Cell 2 ($V_{WL2}$)</th>
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<tbody>
<tr>
<td>On (V)</td>
<td>&gt; 0.9</td>
<td>&gt; 0.9</td>
</tr>
<tr>
<td>Off (V)</td>
<td>&lt; 0.7</td>
<td>&lt; 0.7</td>
</tr>
<tr>
<td>Forbidden (V)</td>
<td>0.7/0.9</td>
<td>0.7/0.9</td>
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Retention time - Charge locking

Discharge circuit - RC

\[ V_G(t) = V_{\text{final}} \left[ 1 + \frac{R_F}{R_G} \exp \left( -\frac{t}{\tau} \right) \right] \]

Time Constant

\( \tau = 0.25-1 \text{ s} \)

Retention time

\( t=20 \text{ ms (voltage drop 1\%)} \)

By operating at high \( V_{WL}^{\text{LOW}} = 0.5V \)
Time multiplexing

Time multiplexing

Conclusion

We are combining three elements that most likely will play a role in a scalable silicon-based quantum processor

- Quantum dots – Quantum electronics
- FETs - Digital electronics
- Gate-based sensing – Analogue electronics

Further steps

- Optimization: Minimization of charge injection and clock feedthrough
- Combination of time and freq multiplexing
- Demonstration of reduction of inputs (3x3)
- IC manufacturing
Thank you for your attention

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